

*Cont'd  
A<sup>2</sup>*  
the sensor TFT area B, the storage area C, and the switching TFT area D. An amorphous silicon is deposited on the substrate 10, and then patterned such that a sensor semiconductor layer 20a and a switch semiconductor layer 20b are formed on the first insulating layer 18 corresponding to the sensor TFT area B and the switching TFT area D, respectively.

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